REMARKS

Claims 1-8 are pending.

Claims 1-8 are rejected.

I. REJECTION UNDER 35 U.S.C. § 102

The Examiner rejected Claims 1-8 under *35 U.S.C. § 102(e)* as being anticipated by U.S. Patent No. 6,791,171 to *Mok et al.* (hereafter "*Mok*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

The invention of *Mok* is directed to the field of integrated circuit (IC) packaging and wafer design, as well as to the fields of interconnection, testing and burn-in structures and processes. More particularly, the invention relates to improvements in photolithography-patterned spring contacts and enhanced system interconnect assemblies having photolithography-patterned spring contacts for use in the testing or burn-in of integrated circuit wafers, and for interconnecting a large number of signals between electronic systems or subsystems.

The present invention is directed towards a method and apparatus wherein a production module, designed to package a production level IC, may be used to test functional sub-sets of the circuitry making up the IC using the production module rather than designing a special test module which may have reduced performance and additional cost. The method of Claim 1 does not require the module to have any particular contact design for connecting an IC chip to a packaging module.

Claim 1 recites a method for testing the design of an integrated circuit (system IC) comprising 7 steps.

1) Designing the system IC to have a predetermined number and pattern for its chip I/O pads. All IC chips are designed to conform to this step.

2) Designing a packaging module to fan-out the I/O of the system IC to an expanded pitch of packaging I/O pads having a correspondence to said chip I/O pads. All IC chips are designed to conform to this step.

3) Partitioning circuitry of said system IC into a functional circuit. The Examiner states that *Mok* discloses this step and cites *Mok* FIGS. 16-21, column 18 lines 36 to column 20 lines 24. *Mok* describes Figs. 16-21 as follows:

FIG. 16 is a plan layout view of an integrated circuit having stress metal springs connected to IC pads and extending from the substrate surface. FIG. 17 is a partial cutaway view of an integrated circuit having looped stress metal springs connected to IC pads and extending from the substrate surface, wherein a portion of the stress metal springs are embedded within a support substrate. FIG. 18 is a side view of integrated circuit devices on a semiconductor wafer. FIG. 19 is a side view of a semiconductor wafer having integrated circuit devices, which is mounted to a compliant wafer carrier substrate. FIG. 20 is a side view which shows the separation between integrated circuits for a semiconductor wafer which is mounted to a compliant wafer carrier substrate and FIG. 21 is a side view showing separated integrated circuits on a compliant wafer carrier substrate which is mounted to a test fixture. Nowhere does *Mok* disclose partitioning circuitry of the system IC into a functional circuit as recited in step 3 of Claim 1. Further *Mok* only mentions functional with respect to testing and functional with respect to schematic of the pattern generation and stimulus/response system architecture in his entire disclosure. The Examiner fails to specifically point out where *Mok* discloses step 3 of Claim 1 as is required by 37 CFR 1.104(c) (2). If *Mok* does disclose this step, then why does the Examiner cites 5 drawings and 3 columns of disclosure none of which recites partitioning circuitry of an IC into functional circuitry. The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation since nothing particular in *Mok* is pointed out as disclosing step 3 of Claim 1.

4) Designing the functional circuit as a corresponding test IC, wherein said test IC I/O pads conform to one of a sub-set of the number and pattern of the chip I/O pads. In this step, the present invention designs the functional circuit as a test IC and makes the I/Os of the test IC conform to a sub-set of existing pad pattern for the production IC.

Mok is doing wafer level testing of single or multiple production level ICs before they are diced up and ready for individual modules. Nowhere does *Mok* mention a test IC because *Mok* is doing wafer level testing of individual IC chips and not partitioning the IC chips into a functional circuit with a sub-set of the number and pattern of the chip(IC) I/O pads and then designing a test IC that corresponds to the functional circuit. The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation since nothing particular in *Mok* is pointed out as designing the functional circuit as the test IC of Claim 1.

5) Attaching the test IC (of step 4) to the packaging module with conductive material. Since *Mok* does not design the test IC of step 4, *Mok* does not attach the test IC to the packaging module designed for the complete IC. The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation since nothing particular in *Mok* is pointed out as attaching the test IC Claim 1 to the packaging module.

6) Exercising said test IC by applying signals and power to inputs of said packaging module at packaging I/O pads corresponding to said sub-set of chip I/O pads. Since *Mok* does not design the test IC of step 4, then it follows that *Mok* does not apply signals to the packaging module as recited in this step.

7) Collecting test data corresponding to said test IC. Since *Mok* does not design the test IC of step 4, then if follows that *Mok* does not collect data corresponding to the test IC of Claim 1.

The Examiner failed to point out one specific element (by number) of Claim 1 in the Figs. of *Mok* or one phrase that recited the steps of Claim 1, in particular steps 4-7. The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically point out where *Mok* teaches the steps of Claim 1 as required by *37 CFR §1.104(c) (2).* Therefore, the Applicant asserts that the rejection of Claim 1 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above arguments.

Claim 2 is directed to a method for testing the design of an integrated circuit (system IC) comprising 8 steps.

1) Designing said system IC to have a predetermined number and pattern for its chip I/O pads.

2) Designing a packaging module to fan-out the chip I/O to an expanded pitch of packaging I/O pads having a correspondence to said chip I/O pads.

3) Partitioning functionality of said system IC into a plurality of individual functional circuits.

4) Designing said plurality of individual functional circuits as a corresponding plurality of test ICs, wherein each of the test ICs conforms to one of a plurality of sub-sets of chip I/O pads making up said number and pattern of said chip I/O pads.

5) Attaching said plurality of test ICs to said packaging module with conductive material.

6) Interconnecting an I/O of a first test IC of said plurality of test ICs to an I/O of a second test IC of said plurality of test ICs external to said packaging module.

7) Operating said plurality of test ICs by applying signals and power to selected ones of said packaging I/O pads corresponding to said plurality of sub-sets of said number and pattern of said chip I/O pads.

8) Collecting test data corresponding to operating said plurality of test ICs.

The Examiner states that *Mok* discloses these steps and cites multiple Figs. of *Mok* without pointing out a single element (by number) that the Examiner believes corresponds to the elements in Claim 2. Likewise, the Examiner cites long, multiple column disclosure of *Mok* without specifically making a correspondence between a particular phrase or sentence of *Mok* that he believes corresponds to the steps of Claim 2.

For step 1, "designing said system IC to have predetermined number and pattern for its chip I/0 pad" the Examiner cites 5 Figs. and 2 columns of disclosure of *Mok* without pointing out anything specific. For step 2, "designing a packaging module to fan-out the chip I/0 to an expanded pitch of packaging I/0 pads having a correspondence to the chip I/0 pads" the Examiner cites 3 Figs. and 2 columns of disclosure of *Mok* without pointing out anything specific. For step 3, "partitioning functionality of the system IC into a plurality of individual functional circuits" the Examiner cites 5 Figs. and

3 columns of discloser of *Mok* without pointing out anything specific. For step 4, "designing the plurality of individual functional circuits as a corresponding plurality of test ICs, wherein each of the test ICs conforms to one of a plurality of sub-sets of chip I/0 pads making up said number and pattern of said chip I/0 pads the Examiner cites 4 Figs. and 4 columns of discloser of *Mok* without pointing out anything specific. For step 5, "attaching said plurality of test ICs to said packaging module with conductive material" the Examiner cites 4 Figs. and 4 columns of disclosure of *Mok* without pointing out anything specific. For steps 6, "interconnecting an I/0 of a first test IC of said plurality of test ICs to an I/0 of a second test IC of said plurality of test ICs external to said packaging module" the Examiner cites 4 Figs. and 4 columns of disclosure of *Mok* without pointing out anything specific. For step 7, "operating said plurality of test ICs by applying signals and power to selected ones of said packaging I/0 pads" the Examiner cites 2 Figs. and 2 columns of disclosure of *Mok* without pointing out anything specific. For step 8, "collecting test data corresponding to operating said plurality of test ICs" the Examiner cites 2 Figs. and 2 columns of disclosure of *Mok* without pointing out anything specific.

The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically point out where *Mok* teaches the steps of Claim 2 as required by *37 CFR §1.104(c) (2)*. Therefore, the Applicant asserts that the rejection of Claim 2 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above argument and for the same reasons as Claim 1.

Claim 3 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 3 adds the 3 steps:

1) Redesigning a first test IC of said plurality of test ICs generating a redesigned first test IC in response to said test data.

2) Replacing a corresponding one of said plurality of test chips with said redesigned first test IC.

3) Repeating steps (e) – (g).

The Applicant has shown that the Examiner failed to make a *prima facie* case of anticipation of Claim 2 for failing to specifically point out where the steps of Claim 2 appear in *Mok*. The Examiner states that *Mok* teaches Claim 3 and cites 4 Figs. and 4 columns of disclosure of *Mok* without pointing out anything specific relative to the 3 steps of Claim 3.

The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically point out where *Mok* teaches the steps of Claim 3 as required by *37 CFR §1.104(c) (2)*. Therefore, the Applicant asserts that the rejection of Claim 3 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above argument and for the same reasons as Claim 2.

Claim 4 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 4 adds the step:

1) Redesigning the functionality of the system IC in response to the test data.

The Applicant has shown that the Examiner failed to make a *prima facie* case of anticipation of Claim 2 for failing to specifically point out where the steps of Claim 2 appear in *Mok*. The Examiner states that *Mok* teaches Claim 4 and again cites 4 Figs. and 4 columns of disclosure of *Mok* without pointing out anything specific relative to the step recited in Claim 4.

The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically point out where *Mok* teaches the steps of Claim 4 as required by *37 CFR §1.104(c) (2)*. Therefore, the Applicant asserts that the rejection of Claim 4 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above argument and for the same reasons as Claim 2.

Claim 5 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 5 adds the 2 steps:

1) Coupling said system IC onto a PCB for a system designed to use said system IC.

2) Operating said system IC to emulate at least one function of said system.

The Applicant has shown that the Examiner failed to make a *prima facie* case of anticipation of Claim 2 for failing to specifically point out where the steps of Claim 2 appear in *Mok*. The Examiner states that *Mok* teaches Claim 5 and cites 2 Figs. and 3 columns of disclosure of *Mok* without pointing out anything specific relative to the 2 steps of Claim 5.

The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically point out where *Mok* teaches the steps of Claim 5 as required by *37 CFR §1.104(c) (2)*. Therefore, the Applicant asserts that the rejection of Claim 5 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above argument and for the same reasons as Claim 2.

Claim 6 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 6 adds the step:

1) Testing said system IC in a test fixture desired for said system IC.

The Applicant has shown that the Examiner failed to make a *prima facie* case of anticipation of Claim 2 for failing to specifically point out where the steps of Claim 2 appear in *Mok*. The Examiner states that *Mok* teaches Claim 6 and again cites 3 Figs. and 3 columns of disclosure of *Mok* without pointing out anything specific relative to the step recited in Claim 6.

The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically point out where *Mok* teaches the steps of Claim 6 as required by *37 CFR §1.104(c) (2)*. Therefore, the Applicant asserts that the rejection of Claim 6 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above arguments and for the same reasons as Claim 2.

Claim 7 is an independent claim directed to a test module for a production system IC having a particular number and pattern of chip I/O pads comprising 4 distinct elements. The Examiner states that *Mok* teaches the invention of Claim 7 and cites the following:

1) For the test IC corresponding to a sub-set of a total functionality of said system IC, said test IC having a test IC I/0 configuration corresponding to a sub-set of said particular number and pattern of chip I/0 pads the Examiner cites *Mok* Figs. 1-4 and column 14 lines 54 through column 15 line 45. The Examiner cites 5 Figs. and 3 columns of *Mok* as teaching the test IC of Claim 7 without specifically pointing out anything specific relative to the test IC recited in Claim 7 as required by *37 CFR §1.104(c) (2).*

2) For the packaging module designed for said production system IC, having a packaging I/0 number and pattern of packaging I/0 pads for receiving said particular number and pattern of chip I/0 pads the Examiner cites *Mok*, Figs. 15-17 and column 18 lines 15 through column 19 lines 19. The Examiner cites 5 Figs. and 3 columns of *Mok* as teaching the test IC of Claim 7 without specifically pointing out anything specific relative to the test IC recited in Claim 7 as required by *37 CFR §1.104(c) (2).*

3) For the couplings for electrically coupling said test IC I/0 configuration to selected ones of said packaging I/0 pads corresponding to said sub-set of said particular number and pattern of chip I/0 pads, the Examiner cites *Mok*, Figs. 54, 55, 75, 76 and column 34 lines 65 through column 37 lines 21. The Examiner cites 4 Figs. and 4 columns of *Mok* as teaching the first couplings of Claim 7 without specifically pointing out anything specific relative to the first couplings recited in Claim 7 as required by *37 CFR §1.104(c) (2).*

4) For the couplings for electrically coupling test signals to said selected ones of said packaging I/0 pads corresponding to said sub-set of said particular number and pattern of chip I/0 pads, the Examiner cites *Mok*, Figs. 54, 55, 75-78 and column 34 lines 65 through column 38 lines 21). The Examiner cites 4 Figs. and 5 columns of *Mok* as

teaching the second couplings of Claim 7 without specifically pointing out anything specific relative to these second couplings recited in Claim 7 as required by *37 CFR §1.104(c) (2)*.

The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically point out where *Mok* teaches the elements of Claim 7 as required by *37 CFR §1.104(c) (2)*. Therefore, the Applicant asserts that the rejection of Claim 7 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above arguments.

Claim 8 is an independent claim directed to a test module for a production system IC having a particular number and pattern of chip I/O pads comprising 4 distinct elements not specifically recited in Claim 7. The Examiner failed to specifically address Claim 8 and rejected Claim 8 for the same reasons as Claim 7 while citing the same references in *Mok* for the elements of Claim 8 as he did for the elements of Claim 7.

The Applicant asserts that the Examiner fails to make a *prima facie* case of anticipation for failing to specifically addressing the limitations of Claim 8 and for the same reasons as Claim 7. Therefore, the Applicant therefore asserts that the rejection of Claim 8 under *35 U.S.C. § 102(e)* as being anticipated *Mok* is traversed by the above arguments.

III. CONCLUSION

The rejections of Claims 1-8 under *35 U.S.C. § 102(e)* over *Mok* have been traversed.

The Applicant, therefore, respectfully assert that Claims 1-8 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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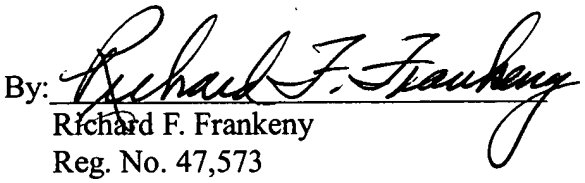
By: 

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